Remarks

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The new title and abstract respectively conform to the claimed invention and the disclosure. The specification amendment corrects the application number of the cited patent application.

The new claims better define the claimed invention.

Claim 6 defines an integrated circuit comprising logic circuitry and first and second scan path segments.

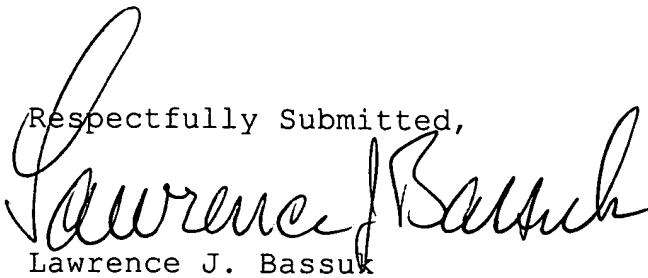
A cache bit memory having a data input and a data output is connected in series between the scan in lead and the scan input of the first scan path segment. The cache bit memory has a scan clock input connected to the scan clock input of the first scan path segment.

US 5,768,289 to James discloses by-passing selected ones of boundary scan cells with control signals in first or second states. In one embodiment depicted in Figures 5 and 6, the by-pass signals for one set of boundary scan cells come from another set of boundary scan cells.

Claim 6 requires a cache bit memory connected in series between the scan in lead and the scan input of the first scan path segment. The cache bit memory has a scan clock input connected to the scan clock input of the first scan path segment. These limitations distinguish over the disclosure in the James patent.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,



Lawrence J. Bassuk
Reg. No. 29,043
Attorney for Applicant

Texas Instruments Incorporated
P. O. Box 655474, MS 3999
Dallas, Texas 75265
972-917-5458